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PATENT APPLICATION

ATTORNEY DOCKET NO. 200301919-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Kevin B. Leigh et al.

Confirmation No.: 2616

Application No.: 09/872,600

Examiner: Huynh, Kim T.

Filing Date: June 1, 2001

Group Art Unit: 2112

Title: SYSTEM AND METHOD OF AUTOMATICALLY SWITCHING CONTROL OF A BUS IN A PROCESSOR-BASED DEVICE

Mail Stop Appeal Brief - Patents
Commissioner For Patents
PO Box 1450
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TRANSMITTAL OF REPLY BRIEF

Transmitted herewith is the Reply Brief with respect to the Examiner's Answer mailed on July 17, 2006 .

This Reply Brief is being filed pursuant to 37 CFR 1.193(b) within two months of the date of the Examiner's Answer.

(Note: Extensions of time are not allowed under 37 CFR 1.136(a))

(Note: Failure to file a Reply Brief will result in dismissal of the Appeal as to the claims made subject to an expressly stated new ground rejection.)

No fee is required for filing of this Reply Brief.

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Respectfully submitted,

Kevin B. Leigh et al.

By 

David M. Hoffman

Attorney/Agent for Applicant(s)

Reg No.: 54,174

Date: September 15, 2006

Telephone: (281) 970-4545

Rev 10/05 (ReplyBrf)

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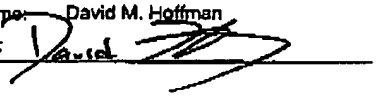
Signature: 

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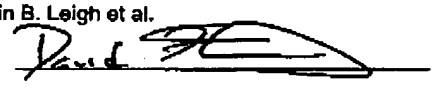
By 

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kevin B. Leigh et al.	§	Group Art Unit: 2112
Serial No.: 09/872,600	§	Examiner: HUYNH, KIM T
Filed: June 1, 2001	§	
For: SYSTEM AND METHOD OF AUTOMATICALLY SWITCHING CONTROL OF A BUS IN A PROCESSOR-BASED DEVICE	§	Atty. Docket: COMP:0213/FLE (200301919-1)

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David M. Hoffman

Mail Stop Appeal Brief-Patents
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Sir:

REPLY BRIEF PURSUANT TO 37 C.F.R. § 41.41 AND IN RESPONSE TO THE EXAMINER'S ANSWER MAILED JULY 17, 2006

This Reply Brief is being filed pursuant to 37 C.F.R. § 41.41 and in response to the Examiner's Answer mailed on July 17, 2006. Specifically, this Reply Brief addresses the Examiner's continuing pattern of misinterpretation of the cited references and the pending claims. However, in the interest of brevity, Appellants address below only those issues or arguments raised by the Examiner's Answer that are most deserving of comment. In view of Appellants' attempt to avoid repetition in this reply, Appellants respectfully request that the Board consider Appellants' complete arguments set forth in the previously filed Appeal Brief regarding issues that have not been addressed again via this Reply Brief.

The Alexander Reference Does Not Disclose Automatically Isolating the First Bus Controller

As described in the Appeal Brief filed on April 13, 2006, one of the claim features of the pending claims absent from the cited references is "automatically isolating the first bus controller from the bus in response to the detection signal." Application, claim 1; *see* Appeal

Brief, pages 12-14. The Examiner has conceded that this feature is absent from the Vivio reference and instead has alleged that the Alexander reference discloses it. Final Office Action, page 2. Appellants responded to this allegation in the Appeal Brief by explaining to the Examiner that none of the bus masters described in the Alexander reference are ever isolated from a bus. *See, e.g.,* Appeal Brief, pages 12-14.

On page 18 of the Examiner's Answer, in the "Response to Argument" section, the Examiner responded to Appellants' explanation by asserting that "when the PCI bus controller [of Alexander reference] gives control to one of the masters, the other masters are prevented from communicating with the disk controller and are thus 'isolated' from it." Appellants do not dispute this interpretation by the Examiner. However, isolating the disk controller 110 from the other masters is *wholly different* from "isolating the first bus controller *from the bus*" as recited in claim 1, for example. (Emphasis added). Contrary to what is recited in the claims, neither the disk controller 110, the controller 107, nor the other masters *are ever isolated from the bus*. Alexander, col. 3, lines 38-52. Although the Examiner is correct that the other masters are prevented from communicating with the disk controller 110 over the bus, the Alexander reference explicitly states that the controller 107 maintains access with the disk controller 110 *over the bus. Id.; see also* Fig. 1. In other words, the disk controller 110 is never isolated from the bus, because it is configured to *communicate with the controller 107 over the bus. See id.* The fact that the disk controller 110 is coincidentally isolated from the other masters is irrelevant, as the disk controller 110 *is not isolated from the bus*, as claimed.

Regardless, Appellants also respectfully assert that the isolation or non-isolation of the disk controller 110 is itself irrelevant, because the disk controller 110 is not a "first bus controller," as recited in claim 1, for example. One of the purposes of the system set forth in the Alexander reference is to prevent "lost data or data collisions resulting from simultaneous control of disk controller 110 *by multiple bus masters*." Alexander, col. 2, lines 54-57 (emphasis added). In other words, the Alexander reference is directed towards a system that prevents two different bus controllers from giving conflicting instructions *to* the disk controller 110. *Id.* Consequently, it would be incorrect to consider the disk controller 110 to be a bus controller, because it is clearly a device that is being *controlled*. If, as the Examiner

alleges, the disk controller 110 were a bus controller, there would be no need in the Alexander reference to arbitrate amongst multiple bus controllers, because the disk controller 110 would be its own controller. For at least these reasons, it is clear that the Examiner's rejection is based upon a misinterpretation of the Alexander reference, which cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103.

Modifying the Vivio Reference as Suggested by the Examiner Would Change the Principle Operation of the Vivio Reference

In the Appeal Brief, Appellants also asserted that it is improper for the Examiner to modify the Vivio reference in view of the Alexander reference, because the modification would change the principle operation of the Vivio reference. *See* Appeal Brief, pages 17-18. The Vivio reference is directed towards a system that enables a computer to operate with either a single processor 122 or with two processors 122 and 128 operating in conjunction, but not with two incompatible processors. Vivio, Figs. 2-4. In other words, the Vivio reference discloses a "one or both" system. However, modifying the Vivio reference as suggested by the Examiner would *prevent the system from ever operating with dual processors*, because the insertion of the second processor 128 would automatically isolate the first processor 122 from the system. In other words, modifying the system as suggested by the Examiner would create a "one or the other system." This modification, however, is improper as modifying the Vivio reference to act as a "one or the other" system would stop dual processor operation and, thus, change the entire operating principle of the Vivio reference. For this reason, the Examiner's rejection is improper and cannot establish a *prima facie* case of obviousness.

In the "Response to Argument" section of the Examiner's Answer, the Examiner responded to Appellants' position by alleging that:

> The Vivio reference is not limited to embodiments wherein processors operate in conjunction with one another. Vivio specifically contemplates the use of different microprocessors (col. 6, lines 23-26), which may or may not be designed to operate in conjunction. Accordingly, isolating these processors in accordance with the teachings of Alexander, III et al. does not render Vivio unsatisfactory for its intended purpose.

Examiner's Answer, pages 19-20.

Appellants, however, respectfully assert that these statements by the Examiner are *factually and technically inaccurate*. As the title of the Vivio reference suggests, the Vivio reference is directed towards a "system for automatic reconfiguration termination to *multi-processor bus* without added expense of removable termination module." Vivio, Title (emphasis added). In other words, as stated above, the Vivio reference discloses a "one or both" system *not a* "one or the other" system. *See* Vivio, col. 4, lines 19-62; *see also* Figs. 2-5. More specifically, in the Vivio system, a first processor (*e.g.*, P6 122 from Fig. 2) is always employed and a second processor (*e.g.*, P6 128) may optionally be employed, *but only in conjunction with the first processor*. Vivio, col. 6, line 21-col. 7, line 21.

In fact, there is simply no way that the Vivio reference could function otherwise. As the Examiner has conceded, the Vivio reference discloses no technique for isolating the first processor. *See* Examiner's Answer, page 3. As such, if a second processor is connected to the bus, it *must work in combination* with the first processor, because *two incompatible processor cannot share the same bus*. The only way to make such a configuration possible is to change the entire purpose and operating principle of the Vivio reference away from dual processor operation by adding the very additional functionality that the Examiner has conceded is absent from the Vivio reference – namely isolating the first processor. As described above, however, this addition would complete change the operating principle of the Vivio reference and make it unfit for its intended purpose.

Although the Examiner is correct that the Vivio reference contemplates a variety of processor types (*e.g.*, 80386, I486, Pentium), there is absolutely no suggestion in the Vivio reference that two *different* types of processors may be employed *together*. *See,* Vivio, col. 6, lines 22-44. Rather, the section of the Vivio reference cited by the Examiner is merely clarifying that its dual processor system may be employed to combine other types of processors besides the illustrated P6s. *See* Vivio, col. 6, lines 26-35. For example, two Pentium processors may be employed or two PowerPC processors, and so forth. This section does not state, imply, or suggest that two *incompatible* processors may be employed on the

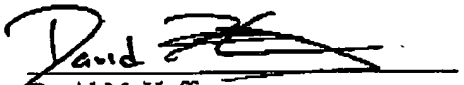
same bus. *See id.* In fact, as described above, and as is notoriously well known in the art, two incompatible processors cannot share a bus. For example, a Pentium processor cannot share a bus with a Power PC, as these processors are incompatible and would constantly conflict with one another. As such, it is clear that the combination of the Vivio and Alexander references is improper. Accordingly, Appellants request withdrawal of the pending rejections and allowance of the present application.

Conclusion

Appellants respectfully submit that all pending claims are in condition for allowance. However, if the Examiner or Board wishes to resolve any other issues by way of a telephone conference, the Examiner or Board is kindly invited to contact the undersigned attorney at the telephone number indicated below.

Respectfully submitted,

Date: September 15, 2006



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